L Number	Hits	Search Text	DB	Time stamp
1	1	("5451551").PN.	USPAT; US-PGPUB	2004/01/05 13:40
2	14	("4417393" | "4486946" | "4701351" | "5011580" | "5091339" | "5116463" | "5118385" | "5137597" | "5142828" | "5164332" | "5173442" | "5211807" | "5219787" | "5380546").PN.	USPAT	2004/01/05 13:30
3	50	5451551.URPN.	USPAT	2004/01/05 13:33
4	266	Planarization	IBM_TDB	2004/01/05 13:41
5	62	Planarization.ti.	IBM_TDB	2004/01/05 13:41
-	10	(("6611060") or ("5412748") or ("5559918") or ("5387815") or ("5426319") or ("5525548") or ("5691222") or ("5872060") or ("6025623") or ("6124553")).PN.	USPAT; US-PGPUB	2004/01/05 09:20
-	40	(("6140208") or ("6162740") or ("6166425") or ("6251786") or ("6294422") or ("6300242") or ("6333248") or ("6333547") or ("6376353") or ("6376386") or ("5466634") or ("5517057") or ("5654567") or ("5898221") or ("5705847") or ("4251852") or ("4322279") or ("4490706") or ("4764804") or ("4769690") or ("4943470") or ("4965660") or ("5188280") or ("5333505") or ("5399527") or ("5506451") or ("5506755") or ("5519254") or ("5532906") or ("5656856") or ("5670801") or ("5683940") or ("5700720") or ("5818699") or ("5916733") or ("5949654") or ("5949097") or ("5981000") or ("6037247") or ("6096630")).PN.	USPAT; US-PGPUB	2004/01/05 09:20
-	6	("5470789" | "5578523" | "5877076" | "5880018" | "5985748" | "6433428").PN.	USPAT	2004/01/05 09:35
-	9	("4663643" | "4782380" | "4931410" | "5081064" | "5082801" | "5153685" | "5234864" | "5306952" | "5341026").PN.	USPAT	2004/01/05 09:39
-	5	("4663643" | "4782380" | "5081064" | "5082801" | "5234864").PN.	USPAT	2004/01/05 09:41
-	4	jp-11102911-$.did. or jp-06275612-$.did.	EPO; JPO; DERWENT	2004/01/05 09:42
-	447	(438/626).CCLS.	USPAT; US-PGPUB	2004/01/05 10:10
-	1753	(438/637).CCLS.	USPAT; US-PGPUB	2004/01/05 10:10

	~~Document ID~~	Pages	Title	Current OR	Current XRef	Inventor
1	US 6297557 B1	11	Reliable aluminum interconnect via structures	257/767	257/758; 257/E21.582; 257/E21.584; 257/E21.585; 257/E23.145; 257/E23.16	Bothra, Subhas
2	US 6114243 A	15	Method to avoid copper contamination on the sidewall of a via or a dual damascene structure	438/687	257/E21.583; 257/E21.584; 257/E21.585; 438/633; 438/638; 438/648; 438/656; 438/666; 438/668; 438/669; 438/671; 438/672; 438/685	Gupta, Subhash et al.

	~~Document ID~~	Pages	Title	Current OR	Current XRef	Inventor
1	US 6670274 B1	7	Method of forming a copper damascene structure comprising a recessed copper-oxide-free initial copper structure	438/692	438/626; 438/633; 438/687; 438/691; 438/699; 438/720; 438/722	Liu, Chi-Wen et al.
2	US 6586326 B2	5	Metal planarization system	438/626	438/687; 438/691	Pallinti, Jayanthi et al.
3	US 6537912 B1	12	Method of forming an encapsulated conductive pillar	438/687	257/E21.011; 257/E21.021; 257/E21.589; 438/626; 438/627; 438/629; 438/637	Agarwal, Vishnu Kumar
4	US 6495200 B1	8	Method to deposit a seeding layer for electroless copper plating	427/97	427/125; 427/98; 438/626; 438/627; 438/643; 438/645; 438/653; 438/672; 438/675; 438/686; 438/687	Chan, Lap et al.
5	US 6417093 B1	12	Process for planarization of metal-filled trenches of integrated circuit structures by forming a layer of planarizable material over the metal layer prior to planarizing	438/626	438/627; 438/633; 438/645; 438/648; 438/687	Xie, James J. et al.
6	US 6184124 B1	15	Method of making embedded wiring system	438/625	438/626; 438/629; 438/631; 438/633; 438/666	Hasegawa, Makiko et al.
7	US 6171928 B1	7	Method of fabricating shallow trench insolation	438/424	257/E21.546; 438/296; 438/436; 438/626; 438/692; 438/693	Lou, Chine-Gie

	~~Document ID~~	Pages	Title	Current OR	Current XRef	Inventor
8	US 6156651 A	23	Metallization method for porous dielectrics	438/674	257/E21.577; 257/E21.581; 257/E21.584; 257/E21.586; 257/E21.587; 257/E23.145; 257/E23.16; 257/E23.167; 438/626; 438/633; 438/675; 438/692	Havemann, Robert H.
9	US 5858874 A	13	Method of fabricating semiconductor device having step of forming plug in contact hole	438/626	257/E21.585; 257/E23.145; 438/629; 438/638; 438/645; 438/666; 438/668; 438/738	Shoji, Hideyuki
10	US 5529955 A	19	Wiring forming method	438/627	257/E21.169; 257/E21.17; 257/E21.295; 257/E21.31; 257/E21.584; 257/E21.585; 438/626; 438/672; 438/683	Hibino, Satoshi et al.
11	US 5472912 A	6	Method of making an integrated circuit structure by using a non-conductive plug	438/643	257/E21.162; 257/E21.295; 257/E21.584; 257/E21.585; 257/E23.019; 257/E23.16; 438/626; 438/627; 438/645	Miller, Robert O.

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12	US 5451551 A	13	Multilevel metallization process using polishing	438/626	216/18; 216/89; 257/E21.582; 257/E21.584; 257/E21.585; 427/124; 427/126.1; 427/248.1; 427/271; 427/307; 427/367; 427/376.7; 427/443.1; 427/96; 438/627; 438/633	Krishnan, Ajay et al.
13	US 20020142581 A1	20	Interconnection structure and method for fabricating same	438/626	257/758; 438/618; 438/622; 438/631; 438/637	Horak, David V. et al.

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1	US 6611060 B1	16	Semiconductor device having a damascene type wiring layer	257/758	257/750	Toyoda, Hiroshi et al.
2	US 6433428 B1	22	Semiconductor device with a dual damascene type via contact structure and method for the manufacture of same	257/750	257/773; 257/E23.158; 257/E23.163	Watanabe, Toru et al.
3	US 6333547 B1	38	Semiconductor device and method of manufacturing the same	257/649	257/E21.293; 257/E21.507; 257/E21.576; 257/E21.577; 257/E21.579; 257/E21.586; 257/E23.019	Tanaka, Masayuki et al.
4	US 5519254 A	8	Multilayer aluminum wiring in semiconductor IC	257/751	257/754; 257/758; 257/763; 257/765; 257/771; 257/E21.582	Tabara, Suguru
5	US 5470789 A	18	Process for fabricating integrated circuit devices	438/643	257/E21.584; 257/E21.585; 438/648; 438/675; 438/687	Misawa, Nobuhiro
6	US 5399527 A	8	Method of forming multilayer aluminum wiring in semiconductor IC	438/625	148/DIG.15; 257/E21.582; 438/659; 438/705	Tabara, Suguru
7	US 5306952 A	26	Multilayer aluminum-containing interconnection structure of semiconductor device	257/165	257/763; 257/E23.145; 257/E23.16	Matsuura, Megumi et al.
8	US 5234864 A	6	Method for interconnecting layers in a semiconductor device using two etching gases	438/694	148/DIG.131; 257/E21.252; 257/E21.311; 257/E21.578; 257/E23.145; 438/700; 438/720; 438/734	Kim, Jin-hong et al.
9	JP 11102911 A	15	SEMICONDUCTOR DEVICE AND ITS MANUFACTURE			HIRAO, HIDEJI

	Document ID	Pages	Title	Current OR	Current XRef	Inventor
10	JP 11102911 A	15	Multilayered wiring connection structure in semiconductor device - includes aluminium film formed for suppressing oxidation of copper film formed on metal wiring			

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1	US 6670268 B2	27	Metal interconnection with low resistance in a semiconductor device and a method of forming the same	438/637	438/586; 438/597; 438/618; 438/622	Shin, Ju-Cheol et al.
2	US 6372633 B1	17	Method and apparatus for forming metal interconnects	438/637	257/763; 257/E21.582	Maydan, Dan et al.
3	US 6313031 B1	7	Method of fabricating a contract structure having a composite barrier layer between a platinum layer and a polysilicon plug	438/643	257/E21.648; 257/E23.145; 438/253; 438/396; 438/637; 438/653; 438/680; 438/681; 438/683	Schuele, Paul J. et al.
4	US 6251774 B1	22	Method of manufacturing a semiconductor device	438/637	257/E21.269; 257/E21.579; 438/622; 438/624; 438/634; 438/638; 438/692; 438/700	Harada, Akihiko et al.